REMARKS

This amendment is responsive to the office action of April 25, 2008, and includes the filing of an RCE.

With regard to the 35 USC 103(a) rejection of claim 73 over Merchant 6,081,523 in view of Shimizu 5,293,378, Allan 5,946,313 and Finney 5,570,356, applicant notes that there are several key differences in structure between applicant's claim 73 and the cited art. Merchant's CRC is computed and verified separately for each segment 22-0 through 22-n of Merchant fig 1, as can be seen in figure 2 (each link having its own CRC checker/generator (col 4 lines 52-53) CRC checker/generator 40-1 for link MII 28-1 is separate and distinct from CRC checker/generator for MII 28-2), and having the function described in Merchant column 5 lines 42-45

> *"CRC field transmitted along a selected one of the MMII links 28 and corresponding physical layer link 22... MII 28-0 may be appended with a CRC field generated based on the continuous stream of nibbles N0, N4, N8 (exclusively the nibbles transmitted on this*

single link) to determine link status and/or link integrity".

In applicant's figure 12, F0 through F3 are a single CRC computed over the entire payload, and not computed on a per-physical link basis as described in Merchant. In Merchant, the corruption of a particular physical link results in a CRC fault to "then decode the generated CRC field to determine whether the corresponding media interface link 21bi and physical layer link 22i provides a reliable connection" (Merchant col 5 lines 45-50). Merchant describes either a CRC which appears on a single lane (fig3A, 3B), or a separate CRC for each data lane (col 5 lines 39-51; col 6 lines 50-58). Applicant has no "corresponding media interface link", as the CRC is computed over the entire payload (not the payload carried exclusively by a particular link) and distributed across all data lanes as presented in claim 73:

"a field check sequence computed over the entire said payload data, concatenated to the end of said payload, and distributed across said n data lanes;"

To draw further distinction, applicant amends the claim to recite "the entire said payload data" to more clearly distinguish from Merchant, which computes the CRC "per physical link".

Applicant also notes that claim 1 recites:

> "A communication interface having n data lanes, said interface sequentially and contiguously transmitting **a header including a packet type field** describing a payload data type, said header distributed across a plurality of said data lanes, a variable amount of payload data comprising an **encapsulated packet having an encapsulated header** and encapsulated data, said payload data distributed across said n data lanes;"

In examiner's office action page 2 8th line from bottom, Examiner has incorrectly indicated the "header including a packet type field" (boldface in claim fragment above) is fig 1 #22 of applicant's invention, anticipated by Merchant's Ethernet packet type of Merchant col 3 line 39 which only describes Ethernet types of packets and not any other types. Applicant's figure 3b (GX Header) identifies a packet type field 64, whereas fig 1 #22 would be the "encapsulated header" (boldface in claim fragment above). Merchant does not teach encapsulation of multiple heterogeneous types of packets (synchronous ATM and asynchronous Ethernet), which, when encapsulated, each of which have their own header types separate and distinct from the GX header which describes a payload type. The "payload

type" of an Ethernet packet is only Ethernet, and is not understood or described to be any other type as recited in claim 1 and described in the examples of applicant's figures 5 through 10 which provide enablement for the claims term "packet type".

With regard to Allen's AAL5 encapsulation of ATM packets into a single Ethernet AAL5 frame, Allen's figure 6A shows the Ethernet packet 3 containing an encapsulated data 14 having a plurality of ATM cell payloads 24 which have their headers removed to form the packet header 44. There is no "encapsulated header present", as the headers 22 have been removed from the ATM cells to form the ethernet packet header 44. This is distinct from applicant's header encapsulation which is independent of the preceding packet header of Allen figure 3B. Applicant's claim 73 describes a packet header followed by a payload which contains an encapsulated header and encapsulated payload, which encapsulated payload is independent of the packet header, and distinguishable from Allen. To draw additional distinction with Allen, applicant amends claim 73 to include:

> <u>"said encapsulated header containing information unrelated to said packet header other than said packet type field;"</u>

thereby reciting a limitation not found in Allen, which has no encapsulated header at all, and derives a packet header address from the payload header.

Applicant's claim 1 is therefore distinct from Merchant and Allen with regard to encapsulation. Applicant has amended claim 1 to recite contiguous transmission, as described in the specification and shown in figure 12:

"said interface sequentially and contiguously transmitting..."

With regard to Shimizu's transmission of END on a data lane, applicant notes that applicant's claim 1 recites function which is simultaneously transmitting either data or synchronizing symbols distributed across all data lanes, whereas Shimizu is a time division multiplexer which transmit SYN patterns at regular time intervals (fig 4A), and begins transmission with SD after an interval asynchronous to SYN, and sends ED when the frame is completed, regardless of SYN. Applicant's invention does not operate in a time divisional multiplexer configuration as described by Shimizu. Therefore, the motivation for Shmizu's SD and ED (indicating frame start and end which are unrelated to fixed interval SYN) is different from applicant's END (indicating a particular data lane for the

end of data. As an illustration of this different motivation, Shimizu figure 2 shows ED on lane 102 which is preceded by no accompanying data at all at any time during this particular time division interval on lanes 103 and 104, a situation which is physically impossible in the system of applicant's claim 1:

> "said header includes transmitting a START symbol on first said data lane, and the transmission of said payload data is **followed by said field check sequence distributed as bytes across said n data lanes and an END symbol on at least one said data lane**;
>
> **said payload data includes transmitting successive data bytes canonically across said n successive data lanes up to data lane m**, where m<=n;"

The organization of data to be transmitted into SYN-SYN intervals (fig 2, 3) by Shimizu also results in the transmission of the start of frame on a next available lane, rather than the first lane, as shown in Shimizu figure 3. Applicant also notes that Shimizu attaches a "sequence number" to each of the transmitted and received frames (col 3 lines 50-60), which is required by Shimizu to preserve the order of transmission, whereas claim 73 describes the order

of transmission by assignment of data lanes and transmission of start frame delimiter on the first data lane.

With regard to Finney, applicant notes that Finney figure 3 teaches a non-sequential distribution of data across lanes compared to applicant's claim 1. Finney distributes data across lanes as "high-byte1, high-byte2, high-byte3, low-byte1, low-byte2, low-byte3" (fig 3 and col 4 lines 33-41). This is not sequential as described in claim 1, which would transmit this data as "high-byte1, low-byte1, high-byte2, low-byte2, high-byte3, low-byte3" which is sequential order, as can also be seen in the byte arrangement of figure 12. Applicant's distribution across lanes is therefore distinct from Finney's distribution.

As neither Shimizu nor Merchant anticipate a header which describes a packet type in a header field which precedes an encapsulated header, a single field check sequence which operates over the encapsulated packet data and is distributed across all of the data lanes, or data distributed sequentially across all lanes, nor distributed as successive data bytes of header, payload, and field check sequence on successive data lanes, applicant's amended claim 73 is allowable. Reconsideration is requested.

With regard to the 35 USC 103(a) rejection of claim 74 over Merchant in view of Shimizu, Allen and Finney,

applicant notes that claim 74 is a proper dependent claim of allowable amended independent claim 73.

With regard to the 35 USC 103(a) rejection of claim 75 over Shimizu in view of Finney and Allen, applicant notes that Shimizu teaches the transmission of synchronization frames in a time division multiplex method with fixed time separation of SYN, where the data is transmitted asynchronously to the SYN markers, and indeed, Shimizu's transmission of payload data is interrupted by the periodic transmission of time division SYN markers (see Fig 2, fig 3, fig 4(a)). Shimizu's motivation for sending time division SYN markers is because his system uses "time division transmission" (col 1 lines 47-48) which divides a transmission interval into equal time length "payload intervals" which are unrelated to the actual duration of transmitted data shown spanning multiple "payload intervals". To draw further distinction from the time division system of Shimizu, applicant's claim 75 is amended to indicate a:

"a first step of sending a synchronization symbol on all four said data lanes until said variable length payload is ready to be transmitted and not sending said

synchronization symbol again until all after all said variable length payload is transmitted;"

and additionally a

"third step of incrementally transmitting the remainder of said payload in an uninterrupted sequence of transmission events...".

As Shimizu's time division transmission requires the periodic transmission of SYN, and SYN is unrelated to the start of frame SD, Shimizu's system is distinguishable from applicant's claim 1 where synchronization symbols are followed by a START delimiter on a first data lane.

With regard to Allen, as described previously with regard to claim 75, the system of Allen figure 3A concatenates a plurality of ATM cells into a single AAL5 payload 14, which strips the header of each ATM cell and forms an AAL header 16 equivalent to the packet header. This is distinguishable from the encapsulated header and encapsulated payload of claim 75, since a plurality of ATM cells rather than just one is encapsulated, and the headers are stripped from ATM cells with identical VPI/VCI to form a new header-less AAL5 payload 2, with an unencapsulated header 40 appearing outside in the header area of the ethernet packet. In contrast, the system of claim 75 has a header (claim 75 second step) which is independent of, and precedes, the "payload having an encapsulated header and

encapsulated payload". The manner of encapsulation of claim 75 which recites a header identifying a payload type which is distinct from the encapsulated header associated with the encapsulated payload is therefore distinguishable from Allen, where there is no encapsulated header at all (Allen figure 3A, header 22 not encapsulated, but put at front of ethernet frame).

Reconsideration is requested.

With regard to the 35 USC 103(a) rejection of claims 76,78,80,82-83,86-89 over Shimizu in view of Finney, applicant notes that Shimizu and Finney do not teach an end symbol on one lane accompanied by a preamble on other lanes, as described in claims 77, 79, 81, 83. Shimizu teaches a preamble on all lanes at times when data is not being sent. Additionally, claims 76,78,80,82-83,86-89 are proper dependent claims which rely on an allowable amended independent claim.

With regard to the 35 USC 103(a) rejection of claim 77, 79, 81 over Shimizu in view of Finney and Allen, applicant notes that amended independent claim 75 is allowable, and claims 77, 79, 81 are proper dependant claims relying on an allowable independent claim.

With regard to the 35 USC 103(a) rejection of claim 84-85, 90 over Shimizu in view of Finney, Allen, and Kimmitt 6,618,395, applicant notes that these are proper dependent claims which rely on allowable independent claim 75.

With regard to the 35 USC 102(b) rejection of claim 91 over Shimizu, applicant notes that examiner's explanation of the operation of Shimizu (found on office action page 14, second paragraph) compared to claim 91 is not correct. Claim 91 recites:

> "sending the remainder of said data stream by sending each subsequent four bytes of unsent data on said first, said second, said third, and said fourth data lanes during successive said time sequences until there is insufficient data to send on all four said data lanes, said insufficient data being final data;"

whereas Shimizu chops the packet into a four time sequential segments a, b, c, and d, and transmits these simultaneously on four different segments. If the stream of data were "a1 ...a8 b1 ... b8 c1 ... c8 d1...d8", then Shimizu would simultaneously transmit "a1 through a8" on lane 101, "b1 through b8" on lane 102, "c1 through c8" on lane 103, and "a1 through a8" on lane 104. In contrast, applicant's claim 75 simultaneously transmits "a1 a5 b1" on a first lane, "a2 a6 b2" on a second lane, "a3 a7 b3" on a third lane, and "a4

a8 b4" on a fourth lane. Structurally, the segmenting of Shimizu requires buffering the entire packet for transmit or receive, whereas applicant's claim 75 distribution only requires buffering 4 data lanes at a time. Claim 91 further recites:

> "when there is no said final data to send, sending said END symbol on said first lane, and said preamble on said second, said third, and said fourth lanes;
>
> when said final data comprises one said data lane, sending said final data on said first lane, an END symbol on said second lane, and said preamble on said third and said fourth lanes;
>
> when said final data comprises two said data lanes, sending said final data on said first and said second lane, an END symbol on said third lane, and said preamble on said fourth lane,
>
> when said final data comprises three said data lanes, sending said final data on said first, said second, and said third lane, and an end symbol on said fourth lane."

Using a similar example as previously shown for this final data, where the stream of final data to be transmitted is "e1 e2 e3", Shimizu transmits "e1 through e3" on one lane and leaves the other lanes empty. This is actually true of

Shimizu not just for "final data" of claim 91 which spans fewer than 4 data lanes, but any amount of data which fits within a time division interval such as e 101 of figure 2. Applicant's claim 91 recites the distribution of final data across the data lanes such that the first lane would carry e1, second lane e2, third lane e3 and END frame on the fourth lane. Shimizu does not operate in this manner, as seen in Shimizu figure 2, in contrast with figure 12 of applicant.

Applicant notes that on page 14 of the office action, examiner includes operational information of Shimizu which is not present at all in this reference. For example, in every drawing example and related description of Shimizu, the frame is interrupted by the required SYN pulse which appears across all frames and is transmitted simultaneously across all segments. **Therefore, and more significantly, Shimizu teaches the transmission of ED at time intervals which are distinct from the transmission of SYN.** However, examiner injects into Shimizu on page 14 of the office action the use of ED on one lane and SYN on the other lanes, which is impossible under Shimizu, as the SYN frames are transmitted together and across all data lanes, and the simultaneous use of ED on one lane and SYN (or final data) on the other lanes is not taught by Shimizu. Examiner further ignores the interruption of packet transmission with

the SYN of all four lanes as indicated in every drawing example of Shimizu - figures 2, 3, 4(a) and 4(b). Shimizu does not teach any of the "final data" combinations of ED and SYN used by examiner in rejecting claim 91, and additionally, the order of segments is completely different than that of claim 91, as described earlier.

With regard to Finney, as described earlier, the transmission order of data B1-HI B1-LO B2-HI B2-LO B3-HI B3-LO B4-HI B4-LO is Lane 1: B1-HI B1-LO; lane 2: B2-HI B2-LO; lane 3: B3-HI B3-LO; and lane 4: G4-HI B4-LO (fig 3 and col 4 lines 33-41), whereas claim 75 recites the sending of a different order, as follows for the same input sequence: lane 1: B1-HI B3-HI; lane 2: B1-LO B3-LO; lane 3: B2-HI B4-HI; lane 4: B2-LO B4-LO. This results in smaller buffer requirements in the present invention claim 91, and Finney's byte mux of figure 2. Reconsideration is requested.

With regard to the 35 USC 103(a) rejection of claims 92-93 over Shimizu in view of Finney, applicant notes that these are proper dependent claims of an allowable independent claim 91.

With regard to the 35 USC 103(a) rejection of claims 94, 95, 96, and 98 over Shimizu in view of Finney, applicant notes that these claims rely on dependent claim 93, which relies on allowable independent claim.

With regard to the 35 USC 103(a) rejection of claim 97 over Shimizu and Finney in view of Widmar, applicant notes that this claim is allowable as being proper and relying on an allowable independent claim.

With regard to the 35 USC 103(a) rejection of claims 100 and 101 over Shimizu and Finney in view of Chung 5,764,895, applicant notes that these claims are allowable as being properly formed and ultimately relying on an allowable amended claim 91.

With regard to the 35 USC 103(a) rejection of claim 102 over Finney in view of Widmar 6,496,540, Shimizu and Allen, applicant notes that amended claim 102 recites different structure and function than Finney. Finney delivers multiple-byte words from each phase to a byte multiplexer which operates on each of the phases (col 2 line 26-27), which byte multiplexer is shown in figure 3 214, storing a high byte and a low byte of data. In particular, incoming data is shown as [HI_BYTE_4 LOW_BYTE_4 HI_BYTE_3 LOW_BYTE_3 HI_BYTE_2 LOW_BYTE_2] which the byte multiplexer 214

organizes for a single lane into HI_BYTE_4 LOW_BYTE_4, whereas claim 102 transmits adjacent data such as [HI_BYTE_4 LOW_BYTE_4 etc on different lanes, as opposed to the same lane as in Finney. For Finney to transmit data on byte boundaries, the byte multiplexer functions 210 and 230 would have to be removed. But Finney describes these as essential elements to practice the invention, as the two bytes are stored to prevent a "buffer underflow" by using "accept 1" etc signals (col 4 line 60 to col 5 lines 1-10). The variation Finney describes and cited by the examiner is "scaling of the number of registers, multiplexers, encoders", but not removal of required elements which would cause a buffer underflow (for example, removal of the byte multiplexer which is fed by the "accept" lines of the serializer is not suggested by Finney). Applicant has amended claim 102 to explicitly recite the transfer of data by the separator as bytes in sequential order across the four data lanes, a feature not found in the non-sequential order of Finney, where a particular lane contains adjacent bytes of data and with four bytes of data being sent simultaneously to the separator at a particular moment in time.

With regard to Finney in view of Shimizu, applicant notes that the motivation for Shimizu's SD and ED is that the data packet of Shimizu is transmitted at a time entirely unrelated to SYN (Shimizu fig 4(a)), and SYN is transmitted

at regular time intervals unrelated to the presence or absence of a packet (figs 3, 4(a), 4(b)), and SYN may interrupt the packet during its transmission (fig 3, fig 4(b)). Since SYN of Shimizu merely establishes time boundaries and has no fixed relationship to the packet, it becomes necessary to introduce SD and ED. This is not the motivation in applicant's invention. Applicant's frame is not interrupted by SYN fields on a single or multiple data lanes. Rather, applicant's START and END provide a redundant method for establishing the beginning and end of a frame which is already bounded by odd and even preamble symbols. Applicant has amended claim 102 to include odd and even preamble symbols in alternating cycles to further distinguish from Finney and Shimizu.

With regard to Shimizu, a transmitter which distributes data across four lanes in Shimizu must have access deep into the transmit buffer at three distant points, indeed the entire packet must be present in the transmit buffer, which is not taught by Finney or present in applicant's claim 102, which delivers data four bytes at a time. The structure required to practice Shimizu requires a transmission buffer 1 containing the entire packet and having access to all parts of the packet, whereas Finney receives a sequence of words which are arranged into bytes. It is therefore not possible to combine Finney and Shimizu as suggested by the examiner. Additionally, the SD and ED delimiters of Shimizu

are not necessary for Finney, as Finney uses the known 8B/10B encoder which includes a "not data" preamble character which is transmitted across all lanes which are not carrying data. The usage of the "not data" preamble character of 8B/10B encoding is commonly used for this purpose in data transmission. Therefore Finney has no functional need for the SD and ED of Shimizu because it relies on the special 8B/10B preamble character "not data" characters. Reconsideration is requested.

With regard to the 35 USC 103(a) rejection of claim 103 over Finney in view of Widmar 6,496,540, Shimizu, and Allen, applicant cancels this claim.

With regard to the 35 USC 103(a) rejection of claim 104 over Finney in view of Shimizu and Allan, applicant notes that the receiver of amended claim 104 recites

> "where said packet header describes said packet payload type but does not include information derived from either said encapsulated header or said encapsulated payload of said packet payload."

whereas the encapsulation of Allen removes headers 22, concatenates payloads 24, and generates a packet header 40. Applicant's amended claim 104 treats encapsulated headers and encapsulated data as separate entities from the packet

header, which only contains information about the type of encapsulation, as claimed. Applicant's amended claim 104 is therefore distinguishable from the combination of Finney and Allen, and Shimizu does not describe encapsulation at all.

With regard to Finney and Shimizu, applicant notes that the receiver of claim 104 does not receive synchronization (non-data) characters in the middle of the payload, and combination of Finney and Shimizu is motivated by the absence of synchronization symbols which are related to the surrounding data, whereas claim 104 recites a clear relationship between synchronization characters which are transmitted before the START and after the END delimiters. Reconsideration of amended claim 104 is requested.

With regard to the 35 USC 103(a) rejection of claims 105-111, applicant notes that these are proper dependent claims which ultimately rely on an allowable independent claim.

With regard to the 35 USC 103(a) rejection of claim 112 over Finney and Kimmitt, applicant notes that the limitation "***the END symbol accompanied by packet data in one lane and preamble in another***," is not found in Shimizu (which transmits ED in one lane and nothing at all in the other lanes), and which does not receive data which is

sequentially four data lanes at a time to form a packet - the data removed from Shimizu has to be wholesale concatenated across entire time division intervals indicated by SYN. The remaining references are silent on the use of delimiters.

With regard to Allen, applicant notes that the demultiplexing shown in figure 6B extracts the VPI/VCI to form the headers of a de-encapsulated packet. In applicant's amended claim 112, the encapsulated header has no relationship to the packet header. Additionally, applicant has added the limitation:

> "where said packet header is unrelated to said extracted encapsulated header, and said packet header only identifies the type of said encapsulated header and said encapsulated packet "

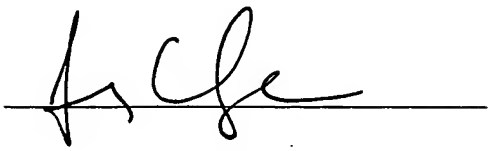
which is additional function and structure distinguishable from Allen. Reconsideration is requested.

With regard to the 35 USC 103(a) rejection of claims 113, 114, 115, 116, 117, 118, 119, applicant notes that these are proper dependent claims which rely on an allowable amended independent claim 112.

With this amendment, this application is in condition for allowance. Examiner is advised that agent Chesavage may

be reached by telephone at 650-619-5270, or via e-mail at patents@chesavage.com

Respectfully Submitted,



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